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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/061,719	
	Filing Date	1/31/02	
	First Named Inventor	Steven Teig, et al.	
	Group Art Unit	2123	
	Examiner Name	<none yet>	
Total Number of Pages in This Submission	*	Attorney Docket Number	SPLX.P0098

Enclosures (Check all that apply)		
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Signature	
Date	January 16, 2004

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PATENT
Docket No. SPLX.P0098

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Mani Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/061,719

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
PERFORMING TECHNOLOGY MAPPING

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This Information Disclosure Statement is submitted within three months of the application filing date or before the mailing date of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

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Dated: January 16, 2004

Respectfully submitted,

By: _____


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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	1	of	2	Application Number	10/061,719
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2123
				Examiner Name	
				Attorney Docket Number	SPLX.P0098

U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	U.S. Patent Document Number Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	2002/0157063 A1	10-24-2002	Besson	
	2.	2002/0178432 A1	11-28-2002	Kim et al.	
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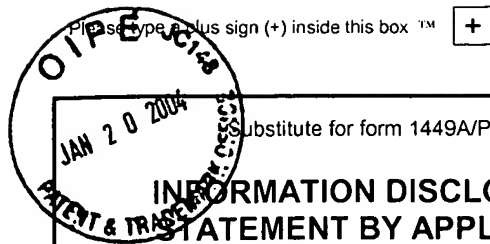
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2123
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Sheet	2	of	2	Attorney Docket Number	SPLX.P0098

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U.S. PATENT DOCUMENTS					JAN 22 2004	
	22.	6,618,835	B1	09-09-2003	Garlapati et al.	Technology Center 2100

NON PATENT LITERATURE DOCUMENTS			
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	23.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).	
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	25.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.	
	26.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.	
	27.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.	

Examiner Signature		Date Considered	
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